**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application:

1-4. (cancelled)

5. (new) A circuit for providing a programmable gain comprising:

a first programmable gain amplifier (PGA) comprising:

an input that receives an input signal to be amplified;

a first plurality of impedances coupled to divide the input signal into a plurality of voltage levels;

a plurality of amplifier circuits coupled to receive the plurality of voltagelevels; and

a first plurality of switches that disconnect each of the amplifier circuits from a power supply, thereby deactivating each amplifier; and

a second PGA configured to receive a voltage level from the first PGA, the second PGA comprising:

a second plurality of impedances coupled to divide the voltage level from the first PGA into a plurality of voltage levels;

and a second plurality of switches that couple said plurality of voltages into a buffer amplifier circuit.

6. (new) The circuit as in claim 5, wherein the first plurality of switches that disconnect each of the amplifier circuits from a power supply, disconnect each amplifier by disconnecting the amplifier from ground.

7. (new) The circuit as in claim 5, wherein the first plurality of switches that disconnect each of the amplifier circuits from a power supply, disconnect each amplifier by disconnecting the amplifier from the power supply voltage.

8. (new) The circuit as in claim 5, wherein the first plurality of switches comprise a plurality of

semi-conductor devices.

9. (new) The circuit as in claim 5, wherein the first plurality of amplifiers comprise a plurality of semi-conductor devices.

10. (new) The circuit as in claim 9, wherein the semi-conductor devices comprise MOS (metal oxide semi-conductor) devices.

11. (new) The circuit as in claim 9, wherein the semi-conductor devices comprise MOS semi-conductor devices.

12. (new) The circuit as in claim 5,wherein the second plurality of switches are semi-conductor switches.

13. (new) The circuit as in claim 12, wherein the semi-conductor switches are MOS devices.

14. (new) The circuit as in claim 5, further comprising a circuit that operates a number of adjacent switches, of the second plurality of switches, concurrently.

15. (new) The circuit as in claim 5, wherein the second plurality of switches further comprises a plurality of switches in parallel that couple the highest voltage level from the second plurality of impedances in the buffer amplifier.

16. (new) The circuit as in claim 5, wherein the second plurality of switches further comprises a plurality of switches in parallel that couple the lowest voltage level from the second plurality of impedances into the buffer amplifier.

17. (new) The circuit as in claim 15, wherein the number of switches in parallel is the same as the number of switches operated concurrently.

18. (new) The circuit as in claim 16, wherein the number of switches in parallel is the same as the number of switches operated concurrently.